REMARKS

INTRODUCTION:

In accordance with the foregoing, claims 1 and 11 have been amended, and new claim 15 has been added. No new matter is being presented, and approval and entry are respectfully requested.

Claims 1-11 and 15 are pending and under consideration. Reconsideration is respectfully requested.

REJECTION UNDER 35 U.S.C. §103:

In the Office Action, at pages 2-5, claims 1-9 and 11 were rejected under 35 U.S.C. §103 in view of Nozuyama (USPN 5,862,359). The reasons for the rejection are set forth in the Office Action and therefore not repeated. The rejection is traversed and reconsideration is requested.

It is respectfully submitted that Nozuyama fails to teach supplying a control signal to a corresponding one of the control signal lines in response to a decoded result of the address information. It appears that the Examiner claims otherwise. In the Response to Argument of the Office Action, the Examiner asserts, "a control signal is supplied from the CPU to a corresponding one of the control signal lines (EN21-EN31, see also column 6, lines 1-46, for example) which are connected to the functional blocks (13, 14, 15, 16, for example) in response to the output of the address decoder 4." The Examiner equates EN21-EN31 to the claimed control signal lines.

In the invention of claims 1 and 11, as amended, a control signal indicative of a write operation or a read operation is transmitted to a corresponding one of the plurality of control signal lines. Such a control signal is completely different from EN21-EN31, which control the coupling/decoupling of the segmented buses. Nowhere in the specification does Nozuyama teach or suggest transmitting a control signal indicative of a write operation or a read operation to a corresponding one of the plurality of control signal lines, which are separate from each other and are connected to the respective function blocks.

In addition, Nozuyama recites, col. 5, lines 51-60:

> Then, each time an appropriate functional block under the condition of the operation speed appears, this functional block should be connected to a predetermined divisional bus with a priority to functional blocks determined in terms of the demand for the achievement of the low power consumption. At any rate, in order to increase the operation speed, it is only natural that a pair of functional blocks which require the most

restricted bus operation speed, should be connected to a divisional bus having the smallest load capacity. (emphasis added)

in the abstract (Nozuyama):

In the low power consumption data transfer bus of the present invention, the mode of division of a bus is associated with a specific layout on an actual LSI chip or an actual LSI-mounted board, and access frequency between functional blocks connected to the bus and therefore the effect of the bus division can be obtained to the maximum degree for the object of achievement of the low power consumption. (emphasis added)

in col. 3, lines 28-47 (Nozuyama):

Loads on the divisional buses 21 to 23 are arranged asymmetrically. Of the plurality of functional blocks 11 to 16, a pair of functional blocks which have the highest average access frequency with respect to the data transfer bus, (for example, CPU and ROM) are connected to one of the divisional buses 21 to 23, which has the smallest load (21 in this embodiment). (emphasis added)

In other words, in FIG. 1, the divisional bus 21, to which a pair of functional blocks which have the highest average access frequency are connected, is constituted so that the load thereon is the smallest under the restriction of the floor layout of the plurality of functional blocks 11 to 16 on the LSI chip 10. (emphasis added)

Hence, it is respectfully submitted that Nozuyama teaches away from the present invention by constraining the choice of functional blocks to be connected by limiting connection for a pair of functional blocks which require the most restricted bus operation speed to a divisional bus having the smallest load capacity and by selecting functional block pairs based on access frequency, which is not recited in amended independent claims 1 and 11 of the present invention.

The Examiner submits (page 5 of the Office Action) that "It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ one instead of two or more functional blocks for each divisional bus, since the use of one functional block instead of two or more functional blocks for each divisional bus is only a matter of design choice." It is respectfully submitted that the courts have held that it is improper to base a rejection on the claimed feature being merely a design choice. See *In re Garrett*, 1986 Pat. App. LEXIS 8 (Bd. Pat. App. 1986), where the U.S. Patent and Trademark Office Board of Patent Appeals and Interferences ("Board") specifically stated: "the examiner has not presented any line of reasoning as to why the artisan would have been motivated to so modify the...structure, and we know of none. The examiner's assertion...that the proposed modification would have been "an obvious matter of engineering design choice well within the level of skill of one of ordinary skill in the art" is a conclusion, rather than a reason." Similar discussions can be seen in *In re Chu*, 36 USPQ2d 1089 (Fed. Cir. 1985).

In addition, the Examiner submitted that "it would have been obvious to one of ordinary

skill in the art at the time the invention was made to employ one instead of two or more functional blocks for each divisional bus is old and well-known as evidenced from Wertheim (previously cited); and using one instead of two or more functional flocks in for each divisional bus in Nozuyama only involves ordinary skill in the art." As noted on page 1, line 37 through page 3, line 3, of the specification, the one to one correspondence of the functional blocks to the destination functional blocks is utilized in the present invention to improve the operation of the semiconductor device. The present application, not the prior art, teaches a one-to-one correspondence.

As described in the present application, conventional semiconductor devices generally connect a plurality of function blocks to a bus. Hence the load on the address/data bus of a conventional semiconductor device increases, causing a need for a high driving performance bus driver, as well as a large number of latch/decoder units, which causes an increase in circuit size. In addition, the greater wire length causes wiring delay, hindering high speed operation and increasing electric power consumption. Also, where more than one function block is connected to a single address/data bus of a conventional semiconductor device, one access operation is effective only for one of the function blocks, thus requiring two cycles by the bus control unit (read, then write) and preventing access and transfer of data between two other function blocks during that two cycle period.

In contrast, the present claimed invention utilizes a bus configuration in which one transferring operation does not require two cycles.

The Examiner cites Wertheim as disclosing the use of one functional block instead of two or more functional blocks for each divisional bus. First, it should be noted that Wertheim is not relied upon in the rejection. Therefore, the teachings of this reference are somewhat irrelevant. Second, it is respectfully submitted that, instead, Wertheim recites a switch controller that controls the states of each of a plurality of switches that connect a plurality of bus segments to different function blocks (see col. 5, line 1 through col. 6, line 36). "A wide variety of switch configurations may be utilized for partitioning buses within the scope of the invention. The switch configuration depends on the bus topology, the bus length and the added circuitry needed for bus partitioning" (col. 5, lines 54-57).

Contrary to the Examiner's interpretation of Nozuyama, it is respectfully submitted that Nozuyama recites three or more divisional buses obtained by dividing the data transfer bus, wherein "the mode of division of a bus is associated with a specific layout on an actual LSI chip or an actual LSI-mounted board, and access frequency between functional blocks connected to

the bus and therefore the effect of the bus division can be obtained to the maximum degree for the object of achievement of the low power consumption. Further the operation speed of the bus (that is, data transfer speed) can be improved as compared to the case where the bus is not divided" (col. 7, lines 25-34). That is, Nozuyama teaches away from the present invention by teaching that the bus is to be divided to provide for achievement of low power consumption based on access frequency such that loads on the divisional buses are asymmetrical, in contrast to the present invention, which recites that the bus division control unit located between the plurality of buses and the main bus is configured to couple one of the plurality of buses to the main bus and to transmit a control signal to a corresponding one of the plurality of control signal lines in response to a decoded result of address information supplied from the bus control unit via the main bus, thereby controlling a corresponding one of the plurality of function blocks, wherein one control signal line is not connected to two or more function blocks.

Thus, claims 1 and 11 are submitted to be patentable under 35 U.S.C. §103(a) in view of Nozuyama (USPN 5,862,359). Since claims 2-4 and 6-9 depend from claim 1, claims 2-4 and 6-9 are submitted to be patentable under 35 U.S.C. §103(a) in view of Nozuyama (USPN 5,862,359) for at least the reasons that claim 1 is submitted to be patentable under 35 U.S.C. §103(a) in view of Nozuyama (USPN 5,862,359).

NEW CLAIM:

New claim 15 recites that the features of the present invention include a semiconductor device comprising: a plurality of function blocks; a plurality of buses, each of which is respectively connected to one of the plurality of function blocks; a plurality of control signal lines, each of which is respectively connected to one of the plurality of function blocks; a main bus; a bus control unit connected to the main bus; and a bus division control unit located between the plurality of buses and the main bus, for connecting a first bus of the plurality of buses to the main bus in accordance with a decoded result of information on the main bus, and controlling a transferring operation between two function blocks connected to a vacant shared second bus of the plurality of buses, and wherein the two function blocks are selected without regard to access frequency.

Nothing in the prior art teaches or suggests such.

It is submitted that this new claim distinguishes over the prior art.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all

pending claims patentably distinguish over the prior art. Thus, there being no further outstanding objections or rejections, the application is submitted as being in condition for allowance which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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